-------------CODE-------------

-----WITHOUT CLK----

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity SHIFT is

Port ( d : in STD\_LOGIC\_VECTOR (3 downto 0);

clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

q :inout STD\_LOGIC\_VECTOR (3 downto 0);

m : in STD\_LOGIC\_VECTOR (1 downto 0));

end SHIFT;

architecture Behavioral of SHIFT is

signal clk\_divider: std\_logic\_vector(23 downto 0);

begin

process(clk,rst)

begin

if rst ='1' then

q<="0000";

elsifclk'event and clk='1' then

---if clk\_divider<= x"3fffff" then

---clk\_divider<= clk\_divider+'1';

---else

---clk\_divider<= x"000000";

case m is

when "00" => q <= d;

when "01" => q <= q (2 downto0)& d(0);

when "10" => q <= d (3) &q(3 downto 1);

when others => q <="0000";

end case;

end if;

end if;

end process;

end Behavioral;

-----WITH CLK---

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

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Port ( d : in STD\_LOGIC\_VECTOR (3 downto 0);

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clk\_divider<= x"000000";

case m is

when "00" => q <= d;

when "01" => q <= q (2 downto0)& d(0);

when "10" => q <= d (3) &q(3 downto 1);

when others => q <="0000";

end case;

end if;

end if;

end process;

end Behavioral;

--------------TEST BENCH CODE------------------

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_unsigned.all;

USE ieee.numeric\_std.ALL;

ENTITY pp\_vhd IS

END pp\_vhd;

ARCHITECTURE behavior OF pp\_vhd IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT SHIFT

PORT(

d : IN std\_logic\_vector(3 downto 0);

clk : IN std\_logic;

rst : IN std\_logic;

m : IN std\_logic\_vector(1 downto 0);

q : INOUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

--Inputs

SIGNAL clk :std\_logic := '0';

SIGNAL rst :std\_logic := '0';

SIGNAL d :std\_logic\_vector(3 downto 0) := (others=>'0');

SIGNAL m :std\_logic\_vector(1 downto 0) := (others=>'0');

--BiDirs

SIGNAL q :std\_logic\_vector(3 downto 0);

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: SHIFT PORT MAP(

d => d,

clk =>clk,

rst =>rst,

q => q,

m => m

);

process

begin

clk<= '0';

wait for 15 ns;

clk<= '1';

wait for 15 ns;

end process;

tb : PROCESS

BEGIN

rst<= '1';

wait for 50 ns;

rst<= '0' ;

d <= "1010" ;

m <= "00";

wait for 100 ns;

m <= "01";

wait for 100 ns;

m <= "10";

wait for 100 ns;

m <= "11";

wait for 100 ns;

-- Wait 100 ns for global reset to finish

wait for 100 ns;

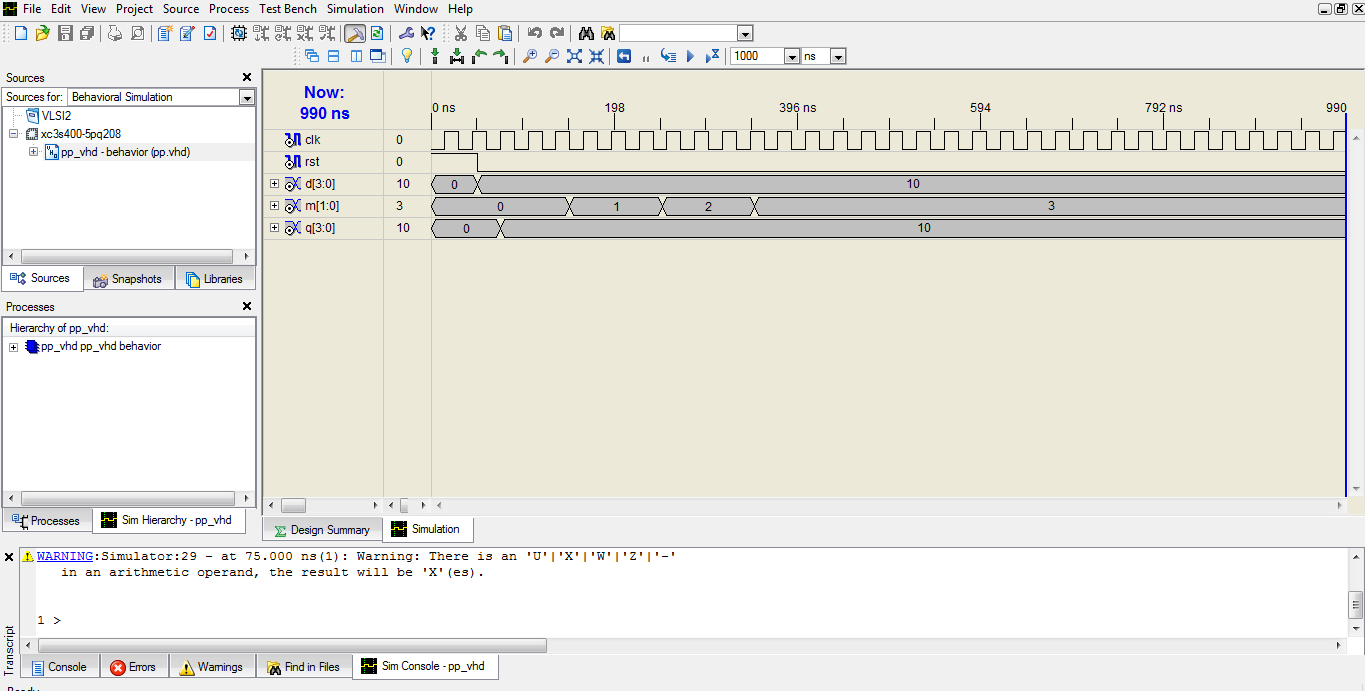
-- Place stimulus here

wait; -- will wait forever

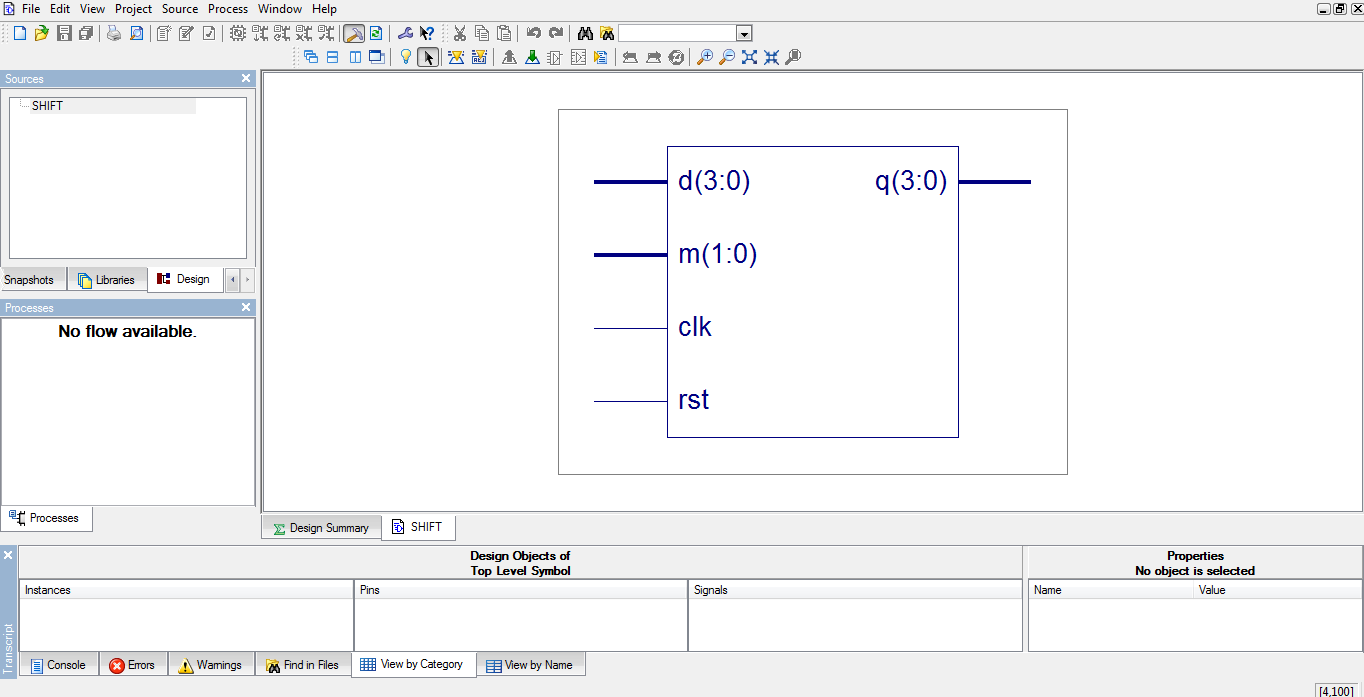
END PROCESS;

END;

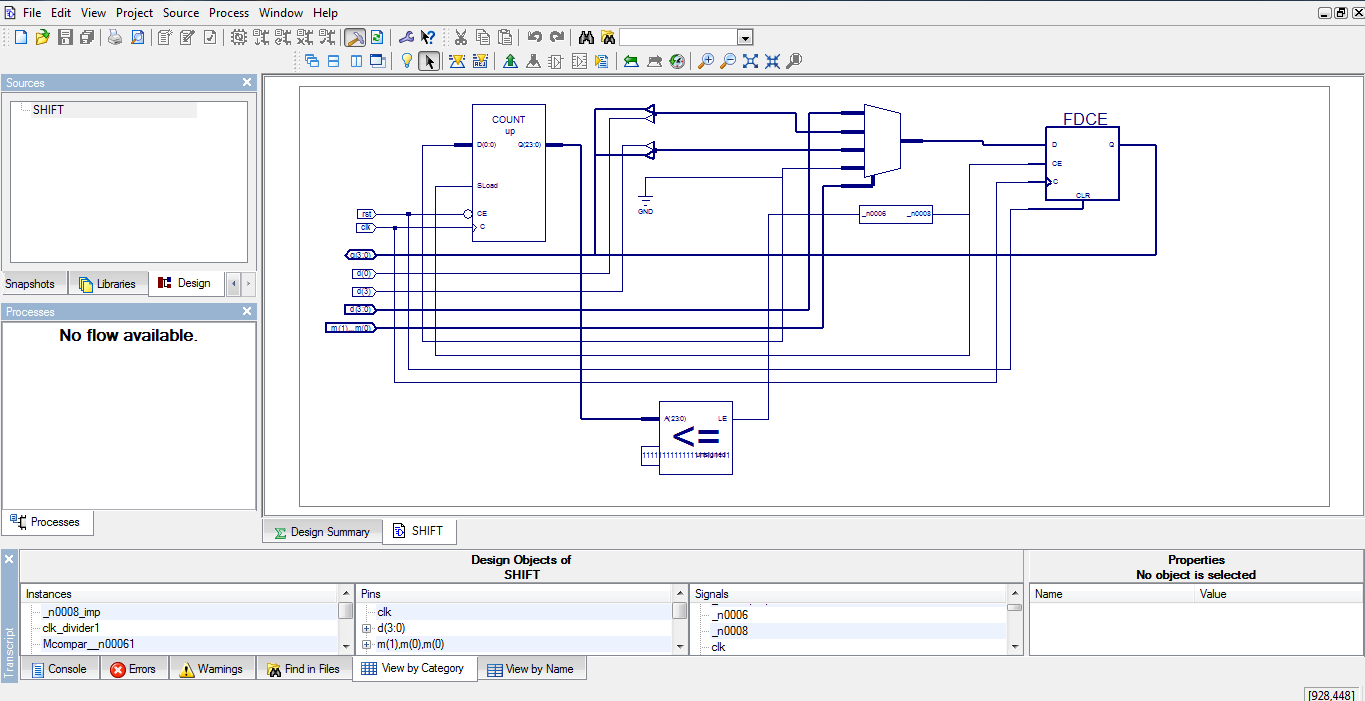
---------------TEST BENCH WAVEFORM-------



------------RTL SCHEMATIC--------------



2.



-------------PIN ASIGNMENT-------------

